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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/813,498	YELURI, SHARADA	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-8,21-24,26,28,30 and 32-36* is/are pending in the application.

4a) Of the above claim(s) *5,9-20,25,27,29 and 31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8,21-24,26,28,30 and 32-36* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-4,6-8,21-24,26,28, 30, 32-36 are presented for examination. Clams 5,9-20,25,27,29,31 have been canceled.

2. Applicant's arguments with respect to claims 1-4,6-8,21-24,26,28, 30, 32-36 have been considered but are moot in view of the new ground(s) of rejection. Rogers et al. (6,357,016) is newly cited reference. However, response by examiner to applicant's reamrks regarding Kurosawa will be included in tis action for clarify the issue.

3. In the remarks, applicant argued that :

4. a) Kurosawa entry numbers are not received in an indication that corresponds to an occurrence of terminating event associated with an instruction ;

5. b) Kurosawa entry numbers were not used to invalidate entry.

6. As to a) Kurosawa's index numbers were indications of the corresponding occurrence of a terminating event associated with an instruction (for terminating events see the memory access instruction completion in col.9, lines 1-7).

7. As to b), Kurosawa taught valid bit , v, in a given entry. Therefore, the entry number had to be known or used in order to validating the correct entry, otherwise the system would have not worked.

The following also included a "101" rejection :

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 1,21 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons are given below.

9. As to claim 1, no physical transformation can be found in the claim. Furthermore, it is not useful because no specific or substantial practical application can be found. The steps associating and receiving are directed to association of the instruction with scoreboard and to provide an indication. The identifying and invalidating is to identify and invalidate the scoreboard. No more details of the receiving, associating , identifying and invalidating can be found in the claim. The unique index in scoreboard may be specific, but it has not substantial practical application, and therefore, not useful. The claim recites "associating instruction", but the instruction is not being stored in a computer readable memory . Therefore, it is not tangible. It is not concrete because no predictable result can be found in the uniquely identified entries. The scoreboard could a table on a design. The evidence shows that applicant also included software logic rather than hardware logic modules (see page 14, last paragraph of applicant's specification). Therefore, it raised a doubt whether applicant is seeking protection for abstract idea or software per se, which is not tangible. Therefore, the claimed invention is directed to non-statutory subject matter. As to claim 21, claim 21 only recites locating step , and invalidating step. No substantial practical application can be found. Similar analysis can be done in claim 21.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1,2,3,8,21, 23,24, 28,30 , 32-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurosawa et al. (5,881 ,264) in view of Rodgers et al. (6,357,016).

11. As to claims 1 , 2,8, 21, Kurosawa disclosed a system with a main memory with a scoreboard comprising at least :

a) associating an instruction (fig.3, col.6, lines 23-36, see also fig.2 for background structure of the scoreboard (11)) with an index (3758ec) into the scoreboard, the index identifying the instruction (READ) ;

b) associating the instruction with a scoreboard entry (No.2) corresponding to the index (see the READ instruction in fig.3);

c) receiving an indication (synchronization) that a terminal event associated with the instruction has occurred (see the memory access instruction completion in col.9, lines 1-7) , the indication including identifying (see the index of READ instruction37s8ecl and invalidating (see the invalid bit entry in fig.3) based on the received scoreboard (see the invalid bit (1) in col.8, lines 4-12, lines 49-53).

12. Kurosawa also including locate an entry in a scoreboard for an instruction with index returned from execution (see col .6, lines 33-52), and invalidating the located

entry (see the set and reset of the flags in scoreboard entry in col.6, lines 47-62, see also the invalidate bit I in the scoreboard entry in fig.3).

13. Kurosawa did not specifically sow the index uniquely identifying the scoreboard entry as claimed. However, Rodgers taught a scoreboard system including entries in a scoreboard each indexed by a unique identifier (see col.12, lines 17-26). It would have been obvious to one of ordinary skill in the art to use Rodgers in scoreboard a index for identifying unique Kurosawa for including the index uniquely identifying the entry as claimed because the use of Rodgers could provide Kurosawa the ability to recognize the particular entry in the scoreboard based on exclusive number of sequence, thereby, minimizing the hardware overheads , therefore the latency, of the scoreboard for identifying the corresponding entries in the system, and because Kurosawa also taught a valid bit for each instruction (see invalid and valid bits in corresponding entries in scoreboard in fig.5), which was a suggestion of the need for provide a unique id, or exclusive index for each valid entry in order to facilitate the unique access of the given entry in the scoreboard, and for doing provided a motivation.

14. As to claim 3, since no specific format of "a load instruction" has been reflected into the claim; the READ instruction is interpreted as a load instruction because a load means reading from memory, a store means writing into memory . As to the long

latency instruction, a read instruction is a long latency instruction because it takes longer time to read from a memory than from a register.

15. As to claim 23, Kurosawa also taught a terminal event (completion) associated with the instruction has occurred (see the memory access instruction completion in col.9, lines 1-7) ,

16. As to claim 24, as to the long latency instruction, a read instruction is a long latency instruction because it takes longer time to read from a memory than from a register.

17. As to claim 28, Kurosawa also included :

a) a scoreboard unit that included plurality of entries (entries) configurable to be indexed with scoreboard indices, the scoreboard unit configurable to indicate in each entry validity information (1) (V) for each instruction (see invalid and valid bits in corresponding entries in scoreboard in fig.5)',

b) an execution unit configurable to maintain scoreboard indices for respective instructions and to scoreboard indices for use for locating and invalidating the respective entries (see the entry numbers in fig.3, see execution in col .6, lines 33-52).

18. Kurosawa did not specifically sow the index uniquely identifying the scoreboard entry as claimed. However, Rodgers taught a scoreboard system including entries in a scoreboard each indexed by a unique identifier (see col.12, lines 17-26). It would have been obvious to one of ordinary skill in the art to use Rodgers in scoreboard a index for identifying unique Kurosawa for including the index uniquely identifying the entry as claimed because the use of Rodgers could provide Kurosawa the ability to

recognize the particular entry in the scoreboard based on exclusive number of sequence, thereby, minimizing the hardware overheads , therefore the latency, of the scoreboard for identifying the corresponding entries in the system, and because Kurosawa also taught a valid bit for each instruction (see invalid and valid bits in corresponding entries in scoreboard in fig.5), which was a suggestion of the need for provide a unique id, or exclusive index for each valid entry in order to facilitate the unique access of the given entry in the scoreboard, and for doing provided a motivation.

19. As to claim 30, Kurosawa also unlocked the entry (order =0) , and stalled the instruction dependent on the operands in the entries (see the order flag in the scoreboard fig.43), locked the entry (order flag = 1) if indicated valid (v) , and unlocked (order flag 0) if invalid (1)).

As to claims 32,33,34, Kurosawa's entry was a register used by respective instruction.

20. As to claim 35, examiner holds that Kurosawa was able to uninstall a dependent instruction because Kurosawa already installed instruction into the scoreboard entries (see the instructions in the scoreboard entries in fig.3).

21. As to claim 36, Kurosawa did not require comparison because it had a valid bit to indicate invalidation of the entry (see the valid flag v).

22. Claims 6,7, 22 ,26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurosawa et al. (5,881 ,264) in view of Rodgers et al. (6,357,016) as applied to claims 1, 21 above, and further in view of Ramagopal et al. (6,473,832).

23. As to claims 6,7,22,26, neither Kurosawa nor Rodgers specifically show the load data has been received nor the forwarding (or receiving) the index value and the instruction to a load / store processing unit as claimed. However, Ramagopal disclosed an indication of load data has been received (col.12, lines 16-63) and a load/store unit (e.g. see fig.1 (26). It would have been obvious to one of ordinary skill in the art to use Ramagopal in Kurosawa for including the indication of load data and forwarding (or receiving) the index value and the instruction to the load/store unit as claimed because the use of Ramagopal could provide Kurosawa the capability of the control circuit to adapt to particular access conditions of a given load or store instruction, thereby reducing the processing overheads of the control processor of Kurosawa, and it could be readily done by configuring the read/write pod of load/store unit of Ramagopal into Kurosawa with modified control! parameters, such as the port width and data type, so that the load store unit of Ramagopal could be recognized by Kurosawa in order to achieve the enhanced system, and for the above reasons, provided a motivation.

24. As to claim 22, Kurosawa also installed instruction into the scoreboard entries (see the instructions in the scoreboard entries in fig.3).

25. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the receiving of the indication that a terminating event associated with the instruction has occurred further comprises receiving an indication that load data Associated with the load instruction has been received.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or

the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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